AMENDMENTS TO THE SPECIFICATION

IN THE ABSTRACT OF THE DISCLOSURE:

Replace the Abstract of the Disclosure currently of record with the attached new Abstract of the Disclosure.

IN THE SPECIFICATION:

Please amend the paragraph beginning on page 1, line 11, with the following amended paragraph:

In these days, an optical recording medium is widely and successfully used for storing various information such as video and audio signals. An optical recording medium is classified into two ~~classes~~ types:[[,]] 'read-only' one such as CD-ROM[[,]] and DVD-ROM, and 'writable' type such as CD-R, DVD-R, CD-R/W, and DVD-RAM.

Please amend the paragraph beginning on page 1, line 16, and continuing to page 2, with the following amended paragraph:

When data is written to a conventional writable optical recording medium, the data is modulated into code matching the recording medium prior to the recording in order to stabilize a servo mechanism in data recording and to stabilize a reproducing clock in data reproduction. Such modulation must satisfy the following constraints ~~that~~: code efficiency is high; a reproducing clock is stable; jitter margin for detecting data stably is ensured; a DC component or digital sum value (DSV) is minimized enough to stabilize data detection and tracking servo; no or the least error propagation arises; and code words have fewer bits as possible as they can.

Please amend the paragraph beginning on page 2, line 14, and continuing to page 3, with the following amended paragraph:

In EFM, one byte, namely, 8 bits are coded to 17-bit symbol data including 3-bit merging bits, and, in EFM+, 8 bits are coded to a 16-bit modulated word depending upon a previous state. The coded data is then converted to NRZI (Non-Return to Zero Inverted) unit which will be written to a writable disk in marks and edges. The distance between successive edges is limited by the rule of RLL (Run Length Limitation), generically designated as RLL(d,k), which means having constraints that at least d 'zeros' are recorded between successive 'ones', and that no more than k 'zeros' are recorded between successive 'ones'. The first constraint arises to obviate intersymbol interference occurring because of pulse crowding of the reproduced ones, which mean transitions, namely ones when a series of 'ones' are contiguously recorded. The second constraint arises to ensure recovering a clock from the reproduced data by locking a PLL to the reproduced transitions.

Please amend the paragraph beginning on page 3, line 2, with the following amended paragraph:

For example, [[In]] in RLL (2,10) used for DVD series, at least two 'zeros' are placed between recorded 'ones', and no more than ten contiguous 'zeros' are placed between recorded 'ones'. Therefore, after NRZI conversion, minimum run length time is (d+1)T and maximum run length time is (k+1)T where T is a channel bit interval. That is, for the example of a (2,10) code, the run length time

ranges from 3T to 11T inclusive.

Please amend the paragraph beginning on page 3, line 9, with the following amended paragraph:

In general, data modulation may use a fixed block scheme in which source data is one-to-one mapped to corresponding modulated data with reference to a conversion table. For this mapping, there is a single conversion table for CD series containing 256 (0 to 255) 16-bit code words ~~for 0 to 255~~ whereas there are four sets of main conversion tables and four sets of sub-tables for DVD series. Each main table contains 256 16-bit code words and each sub-table contains 88 (0 to 87) 16-bit code words ~~for 0 to 87~~. However, in the fixed block scheme, the RLL constraints may be violated between two consecutive bytes under a given code rate even though each byte satisfies the RLL constraints. If the RLL constraints are violated between two successive bytes, one bit must be inserted therebetween. Moreover, one additional bit is added for DC balance. This additional bit for the DC balance demands another one bit to satisfy the given RLL constraints. Therefore, a total of three bits must be inserted if the given RLL constraints are violated between two successive bytes.

Please amend the paragraph beginning on page 3, line 25, and continuing to page 4, with the following amended paragraph:

As described above, [[a]] the fixed block scheme has an advantage of no conversion error because a source data is one-to-one mapped to the corresponding modulated data, whereas it has a drawback in that the recording

density is somewhat limited because of a merging bit and additional bits which are necessary when the given RLL constraints are violated between two consecutive bytes.

Please amend the paragraph beginning on page 4, line 4, with the following amended paragraph:

In the modulation for DVD series, no need for additional bits arises because a previous mapping state is considered at the present mapping process. This modulation is called a 'look-ahead' scheme in comparison with the fixed block scheme. However, there are problems in that mapping algorithm is complicated and many tables are required. The look-ahead scheme is superior to the fixed block scheme in increasing storage capacity. In the look-ahead scheme, the modulation of a current data (symbol) is dependent on next data or previous data occasionally. The look-ahead scheme needs a simple algorithm and hardware and it requires only 2 bits for DC balance as well[[,]]. [[t]]Therefore, it can ensure higher storage capacity of a recording medium than the fixed block scheme.

Please amend the paragraph beginning on page 4, line 16, with the following amended paragraph:

However, the look-ahead scheme has a drawback in that if an error occurs in a certain data, it propagates to subsequent data because the modulation of a current data depends upon the next or previous data.

Please amend the paragraph beginning on page 4, line 19, with the following amended paragraph:

For a high-density writable optical recording medium, new modulating methods are being demanded to ensure stable jitter margin and to increase storage capacity. The new modulating methods have common tendencies <u>in</u> that the code rate is 2/3 to convert an 8-bit source data to a 12-bit code data and (1,7) or (1,8) code is used. In this case, DSV is minimized to stabilize data reproduction and servo mechanism.

Please amend the paragraph beginning on page 5, line 7, with the following amended paragraph:

Therefore, it is desirable to suppress low-frequency components of the coded sequence in order to make a servo irresponsive to low-frequency components. In order to prevent the modulated sequence from containing a DC component, control of DSV has been proposed. The DSV is an indicator of a DC component contained in a train of sequences, and it is a total found by adding up the values of a train of bits, wherein the values +1 and –1 are assigned to '1' and '0' in the train respectively, which results <u>in</u> after <u>the</u> NRZI modulation of a train of channel bits. For example, if a train of bits is "1001000" after <u>the</u> modulation, it is converted to "1110000" by <u>the</u> NRZI modulation. For this sequence, the DSV varies to 1, 2, 3, 2, 1, 0, and -1 sequentially bit by bit.

Please amend the paragraph beginning on page 5, line 19, with the following amended paragraph:

A substantially constant DSV means that the frequency spectrum of the signal does not comprise frequency components in the low frequency zone. The DSV control is accomplished by calculating a DSV of a train of encoded bits after an RLL(d,k) modulation for a predetermined period of time and inserting a predetermined number of DSV control bits into the train of encoded bits. In order to improve the code efficiency, it is desirable to reduce the number of DSV control bits to a smallest possible value.

Please add the following paragraph on page 6 after line 9:

It is another object of the present invention to provide data modulation/demodulation method and apparatus, which overcome the problems and limitations associated with the related art.

Please amend the paragraph beginning on page 6, line 10, with the following amended paragraph:

A method of modulating data to be written onto an optical recording medium in accordance with an aspect of the present invention ~~is characterized in that it~~ comprises the steps of modulating a source data twice based on a first mapping table and a second mapping table wherein the first mapping table contains coded data corresponding to the source data and the second mapping table contains at least one coded data, capable of suppressing low frequency components, to which at least one source data among all source data contained

in the first mapping table is mapped; and selecting one of the modulated data based on at least one among the conditions of the value of a previous source data, the time when low-frequency suppression has been conducted, the value of subsequent modulated data, and whether or not RLL constraints are violated.

Please amend the paragraph beginning on page 6, line 23, and continuing on page 7, with the following amended paragraph:

A method of demodulating coded data read from an optical recording medium in accordance with an aspect of the present invention ~~is characterized in that it~~ comprises the steps of reading a channel data from the optical recording medium, the channel data having been modulated from a source data using a table selected among a plurality of mapping tables based on at least one among the conditions of the value of a previous source data, the time when low-frequency suppression has been conducted, the value of subsequent modulated data, and whether or not RLL constraints are violated; and demodulating the read channel data using a plurality of de-mapping tables in which a decoded data corresponding to the channel data is contained.

Please amend the paragraph beginning on page 7, line 8, with the following amended paragraph:

An apparatus of modulating data to be written onto an optical recording medium in accordance with an aspect of the present invention ~~is characterized in that it~~ comprises a modulator modulating a source data twice based on a first mapping table and a second mapping table wherein the first mapping table

contains coded data corresponding to the source data and the second mapping table contains at least one coded data, capable of suppressing low frequency components, which at least one source data among all source data contained in the first mapping table is mapped to; and a controller selecting one of the modulated data based on at least one among the conditions of the value of the source data, the time when low-frequency suppression has been conducted, the value of subsequent modulated data, and whether or not RLL constraints are violated.

Please amend the paragraph beginning on page 7, line 21, and continuing to page 8, with the following amended paragraph:

An apparatus of demodulating coded data read from an optical recording medium in accordance with an aspect of the present invention ~~is characterized in that it~~ comprises a detector reading a channel data from the optical recording medium wherein the channel data having been modulated from a source data using a table selected among a plurality of mapping tables based on at least one among the conditions of the value of a previous source data, the time when low-frequency suppression has been conducted, the value of subsequent modulated data, and whether or not RLL constraints are violated; and a demodulator demodulating the read channel data using a plurality of de-mapping tables in which a decoded data corresponding to the channel data is contained.

Please amend the paragraph beginning on page 8, line 6, with the following amended paragraph:

The data modulating/demodulating method and apparatus for an optical recording medium in accordance with <u>an aspect of</u> the present invention uses a code rate of 2/3 and the RLL constraints of (1,8).

Please add the following paragraph on page 8, after line 9:

<u>These and other objects of the present application will become more readily apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.</u>

Please amend the header on page 8, line 23 as follows:

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT<u>S</u>

Please amend the paragraph beginning on page 8, line 24, and continuing to page 9, with the following amended paragraph:

The above object<u>s</u> and features of the present invention will be more apparent from the following description of the preferred embodiments with reference to the drawings.

Please amend the paragraph beginning on page 9, line 9, with the following amended paragraph:

In the mapping rule of Table 1, if a source is "00", '1' is inserted between two zeros[[,]]; if a source is "01", '0' is inserted between '0' and '1' in consideration of *d* constraint[[,]]; and if a source is "10" [[and]] or "11", '0' is inserted between '1' and '0' and between two ones, respectively.

Please amend the paragraph beginning on page 13, line 5, with the following amended paragraph:

Figs. 1 to 4 show block diagrams of a data modulating/demodulating apparatus in accordance with an embodiment of the present invention.

Please amend the paragraph beginning on page 13, line 8, with the following amended paragraph:

The apparatus of Fig. 1 comprises an encoding pattern detector/DSV control pointer generator 1, an encoder 2, and a DSV controller 3 which are placed in ~~serial~~ series between a channel and an input line through which a train of source data in entered, all operatively coupled.

Please amend the paragraph beginning on page 13, line 12, with the following amended paragraph:

The encoding pattern detector/DSV control pointer generator 1 receives source data and stores it in a buffer (not ~~figured~~ shown). The stored source data

is sent to the encoder 2 by the encoding pattern detector/DSV control pointer generator 1 together with both a match pattern selecting signal pointing out one among Tables 1 to 7 for mapping a source data and a DSV control pointer indicating whether to conduct DSV control.

Please amend the paragraph beginning on page 13, line 19, and continuing to page 14, with the following amended paragraph:

The encoder 2 determines, based on the match pattern selecting signal, which table to use to map a source data among the 2/3 mapping table 'Table 1', the 4/6 mapping table 'Table 3', the 6/9 mapping table 'Table 5, the 8/12 mapping table 'Table 6', and the 10/15 mapping table 'Table 7'. If the DSV control pointer is received from the encoding pattern detector/DSV control pointer generator 1, the encoder 2 uses Table 2 or 4 for controlling DSV to map a source data. For this modulation, the encoder 2, as shown in Fig. 2, contains look-up tables (LUTs) ~~composed of~~ including the 2/3 mapping table 'Table 1', the 2/3 mapping table 'Table 2' for DSV control, the 4/6 mapping table 'Table 3', the 4/6 mapping table 'Table 4' for DSV control, the 6/9 mapping table 'Table 5', the 8/12 mapping table 'Table 6', and the 10/15 mapping table 'Table 7'.

Please amend the paragraph beginning on page 15, line 19, and continuing to page 16, with the following amended paragraph:

A demodulating device according to an embodiment of the present invention comprises a decoding pattern detector 4 and a decoder 5, as shown in Fig. 1, which are placed in ~~serial~~ series between an output line through which a

train of decoded data is carried and the channel through which a channel bit stream is entered. The decoding pattern detector 4 stores a channel bit stream reproduced from a recording medium into a buffer (not ~~figured~~ shown). The decoding pattern detector 4 sends the stored channel bit stream composed of coded sequence to the decoder 5 and it also provides the decoder 5 with a match pattern selecting signal for each given coded word or sequence. The match pattern selecting signal is indicative of which table is used for de-mapping a given coded word or sequence among Tables 1 to 7.

Please amend the paragraph beginning on page 16, line 4, with the following amended paragraph:

The decoder 5 chooses the 2/3 mapping table 'Table 1', the 4/6 mapping table 'Table 3', the 6/9 mapping table 'Table 5', the 8/12 mapping table 'Table 6', the 10/15 mapping table 'Table 7', the 2/3 mapping table 'Table 2' for DSV control, or the 4/6 mapping table 'Table 4' for DSV control in accordance with the match pattern selecting signal to de-map the coded word or sequence. To conduct this demodulation, the decoder 5 contains LUTs for de-mapping, including ~~composed of~~ the 2/3 mapping table 'Table 1', the 4/6 mapping table 'Table 3', the 6/9 mapping table 'Table 5', the 8/12 mapping table 'Table 6', the 10/15 mapping table 'Table 7', the 2/3 mapping table 'Table 2' for DSV control, and the 4/6 mapping table 'Table 4' for DSV control, as shown in Fig. 4. The decoder 5 does not conduct DSV control operation such as an insertion of DSV control bit because the coded sequence has been modulated in consideration of DSV[[,]]. [[i]]Instead, it simply de-maps the coded word or sequence with

reference to a selected table, e.g., Table 1, 2, 3, 4, 5, 6, or 7.

Please amend the paragraph beginning on page 16, line 27, and continuing to page 17, with the following amended paragraph:

In addition, because the *k* factor in RLL constraints is relatively small, the stable clock restoration is possible, and modulation/demodulation algorithm is simple. ~~and,~~ [[m]] Moreover, an additional DSV control circuit is not necessary, whereby complexity of [[a]] hardware can be reduced remarkably.